

**Computer Architecture Project**

**SEM-Team 10**



**Names**

* **Moamen Hassan**
* **Hussein Youssef**
* **Hassan Osama**
* **Mohamed Magdy**

# **Design**

The Processor is similar to PDP11-based microprocessor that can execute the program loaded in its ram.

The Processer has 3 busses to write data on them. The first Two ‘A’ and ‘B’ can read from registers and The Third ‘C’ can write data into register.

We assume that we have two temp registers ‘X’ and ‘Y’.

**Components**

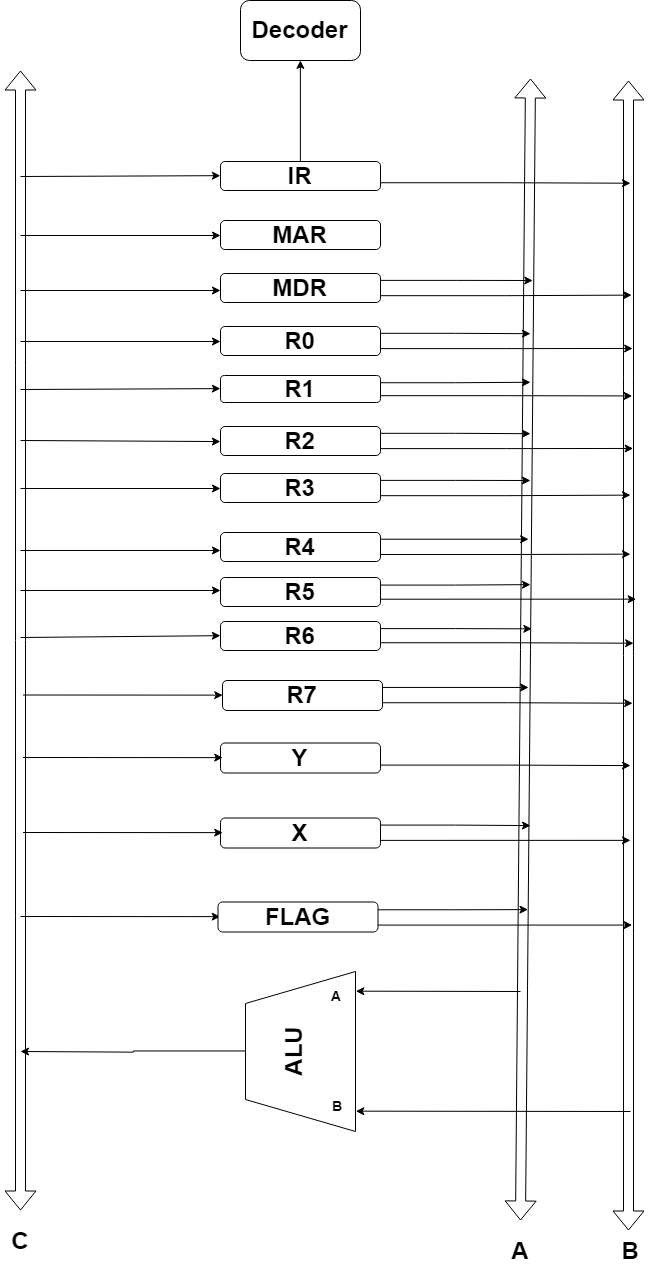
Eight Registers numbered from **R0** to **R7**.

Two temp registers **X**, **Y**.

Four special purpose registers **IR**, **MAR**, **MDR**, **FLAG**.

* **IR**: Instruction Register
* **MAR**: Memory Address Register
* **MDR**: Memory Data Register
* **FLAG**: Status Flag Register contains (**C**, **Z**, **N**, **P**, **O**)
* **C**: Carry Flag.
* **Z**: Zero Flag (1 if ALU result is 0).
* **N**: Negative Flag (1 if ALU result sign is Negative).
* **P**: Parity Flag (1 if ALU result is even).
* **O**: Overflow Flag (1 if P+P=N or N+N=P or P-N=N or N-P=P)

**ALU** that makes operations such as add , sub , addc, subc.



**Mapping the instructions.**

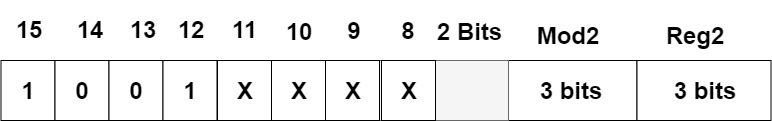
**Two Operand Instructions.**

The selector of the instructions is 4 bits (most 4 significant bits).



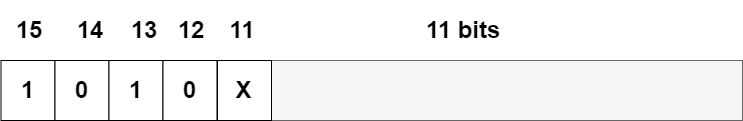
|  |  |
| --- | --- |
| opcode | Two Operand Instructions |
| 0000 | **MOV** |
| 0001 | **ADD** |
| 0010 | **ADC (Add with Carry)** |
| 0011 | **SUB** |
| 0100 | **SBC (Sub with Carry)** |
| 0101 | **AND** |
| 0110 | **OR** |
| 0111 | **XNOR** |
| 1000 | **CMP (Compare)** |

**One Operand Instructions**

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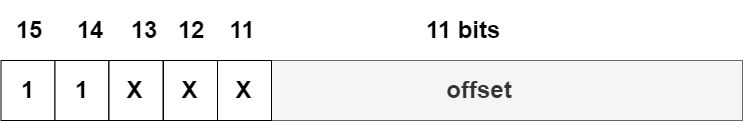
|  |  |
| --- | --- |
| opcode | One Operand Instructions |
| 0000 | **INC (Increment)** |
| 0001 | **DEC (Decrement)** |
| 0010 | **CLR (Clear)** |
| 0011 | **INV (Inverter)** |
| 0100 | **LSR (Logic Shift Right)** |
| 0101 | **ROR (Rotate Right)** |
| 0110 | **RRC (Rotate Right with Carry)** |
| 0111 | **ASR (Arithmetic Shift Right)** |
| 1000 | **LSL (Logic Shift Left)** |
| 1001 | **ROL (Rotate Left)** |
| 1010 | **RLC (Rotate Left with Carry)** |

**No Operand Instructions**

****

|  |  |
| --- | --- |
| opcode | No Operand Instructions |
| 0 | **HLT (Halt)** |
| 1 | **NOP (No Operation)** |

**Branches Instructions**

****

|  |  |
| --- | --- |
| opcode | Branches Instructions |
| 000 | **BR (Branch unconditionally)** |
| 001 | **BEQ (Branch if equal)** |
| 010 | **BNE (Branch if not equal)** |
| 011 | **BLO (Branch if Lower)** |
| 100 | **BLS (Branch if Lower or same)** |
| 101 | **BHI (Branch if Higher)** |
| 110 | **BHS (Branch if Higher or same)** |

**Bonus Instructions**

**1 – JSR Address**

****

**2 – RTS**

****

**3 – IRET**

****

**4 – INTERRUPT**

****

**Addressing Modes**

|  |  |
| --- | --- |
| opcode | Addressing Modes |
| 000 | **Register Mode** |
| 001 | **Auto-Increment** |
| 010 | **Auto-Decrement** |
| 011 | **Indexed** |
| 100 | **Register Mode Indirect** |
| 101 | **Auto-Increment Indirect** |
| 110 | **Auto-Decrement Indirect** |
| 111 | **Indexed Indirect** |

**Analyzing the Design :-**

|  |  |  |  |
| --- | --- | --- | --- |
| **Addressing Mode** | **Instruction** | **Clock Cycles** | **MA** |
| **Register Mode** | **MOV Ro,R1** | **4** | **1** |
| **ADD R3,R5** | **4** | **1** |
| **Auto Increment Mode** | **ADD Ro,(R1)+** | **6** | **3** |
| **AND (R1)+,Ro** | **6** | **2** |
| **Auto Decrement Mode** | **XNOR Ro,-(R1)** | **6** | **3** |
| **OR (R1)+,-(Ro)** | **8** | **4** |
| **Indexed** | **Add X(Ro),R1** | **5** | **3** |
| **SUB X(Ro),(R1)+** | **8** | **5** |
| **MOV X(R0),-(R1)** | **8** | **5** |
| **Register Indirect** | **MOV @(Ro),@(R1)** | **7** | **3** |
|  | **ADD @(Ro),(R1)+** | **8** | **4** |
|  | **Add @(R1),-(Ro)** | **8** | **4** |
|  | **Add @(R1),X(Ro)** | **7** | **5** |
|  | **Add @(Ro),R1** | **5** | **2** |
| **Auto Increment Indirect** | **MOV @(Ro)+,R1** | **6** | **3** |
| **MOV @(Ro)+,(R1)+** | **9** | **4** |
| **ADD @(Ro)+,-(R1)** | **9** | **5** |
| **SUB @(Ro)+,X(R1)** | **8** | **6** |
| **XOR @(Ro)+,@R1** | **8** | **5** |
| **Auto Decrement Indirect** | **CLR @-(Ro)** | **7** | **3** |
|  | **MOV @-(Ro),(R1)+** | **9** | **4** |
|  | **ADD @-(Ro),-(R1)** | **9** | **5** |
| **Indexed Indirect** | **Add @X(Ro), R1** | **9** | **4** |

**Add X(R0) , @R1 (5 MA)**

1. **Instruction Fetch/Decode (3 Cycles)**
2. **PCout A , Transfer A , MARin , Read**
3. **PCout A , F = A+1 , PCin , WMFC**
4. **MDRout A , Transfer A , IRin**
5. **First Operand Fetch (4 Cycles)**
6. **PCout A , Transfer A , MARin , Read**
7. **PCout A , F = A+1 , PCin , WMFC**
8. **MDRout A , R0out B , F = A+B , MARin , Read , WMFC**
9. **MDRout A , Transfer A , Xin**
10. **Second Operand Fetch (1 Cycle)**
11. **R1out A , Transfer A , MARin , Read , WMFC**
12. **Operation and Save (1 Cycle)**
13. **MDRout A , Xout B , F = A+B , MDRin , Write**

**BRQ label (1 MA)**

1. **Instruction Fetch/Decode (3 Cycles)**
2. **PCout A , Transfer A , MARin , Read**
3. **PCout A , F = A+1 , PCin , WMFC**
4. **MDRout A , Transfer A , IRin**
5. **Operation and Save (1 Cycle)**
6. **Address of IRout A , PCout B , F = A+B , PCin (if Z(bar) then END)**

**HALT (1 MA)**

1. **Instruction Fetch/Decode (3 Cycles)**
2. **PCout A , Transfer A , MARin , Read**
3. **PCout A , F = A+1 , PCin , WMFC**
4. **MDRout A , Transfer A , IRin**

**JSR R0 , Routine (3 MA)**

1. **Instruction Fetch/Decode (3 Cycles)**
2. **PCout A , Transfer A , MARin , Read**
3. **PCout A , F = A+1 , PCin , WMFC**
4. **MDRout A , Transfer A , IRin**
5. **Operand (Address) Fetch (3 Cycles)**
6. **PCout A , Transfer A , MARin , Read**
7. **PCout A , F = A+1 , PCin , WMFC**
8. **MDRout A , Transfer A , Xin**
9. **Operation and Save (3 Cycles)**
10. **R6(SP)out A , F = A - 1 , R6in , MARin**
11. **PCout A , Transfer A , MDRin , Write**
12. **Xout A , transfer A , PCin , WMFC**

**CPI = 25 / 4 = 6 Cycles per instruction on Average**

**Grouping**

|  |  |  |  |
| --- | --- | --- | --- |
| **El Out Registers To Bus A** | | **El Out Registers To Bus B** | |
| **1111** | **No Transfer** | **1111** | **No Transfer** |
| **0000** | **R0out** | **0000** | **R0out** |
| **0001** | **R1out** | **0001** | **R1out** |
| **0010** | **R2out** | **0010** | **R2out** |
| **0011** | **R3out** | **0011** | **R3out** |
| **0100** | **R4out** | **0100** | **R4out** |
| **0101** | **R5out** | **0101** | **R5out** |
| **0110** | **R6out** | **0110** | **R6out** |
| **0111** | **R7out** | **0111** | **R7out** |
| **1000** | **FLAGout** | **1000** | **FLAGout** |
| **1001** | **Xout** | **1001** | **Xout** |
| **1010** | **Yout** | **1010** | **Yout** |
| **1011** | **MDRout** | **1011** | **MDRout** |
| **1100** | **IRout** | **1100** | **IRout** |
| **1101** | **Zout** | **1101** | **Zout** |

|  |  |  |  |
| --- | --- | --- | --- |
| **El In Registers From BusC** | | **EL In For Temps** | |
| **1111** | **No Transfer** | **00** | **No Transfer** |
| **0000** | **R0in** | **01** | **Xin** |
| **0001** | **R1in** | **10** | **Yin** |
| **0010** | **R2in** | **11** | **Zin** |
| **0011** | **R3in** |  | |
| **0100** | **R4in** | **EL In For Memory Register** | |
| **0101** | **R5in** | **00** | **No Transfer** |
| **0110** | **R6in** | **01** | **MDRin** |
| **0111** | **R7in** | **10** | **MARin** |
| **1000** | **IRin** |  |  |

|  |  |
| --- | --- |
| **ALU** | |
| **0000** | **Add** |
| **0001** | **Sub** |
| **0010** | **And** |
| **0011** | **OR** |
| **0100** | **XOR** |
| **0101** | **NOT** |
| **0110** | **ROL** |
| **0111** | **ROR** |
| **1000** | **SHL** |
| **1001** | **SHR** |
| **1010** | **RORC** |
| **1011** | **ROLC** |
| **1100** | **ASHR** |
| **1101** | **CLEAR** |
| **1110** | **INC** |
| **1111** | **DEC** |

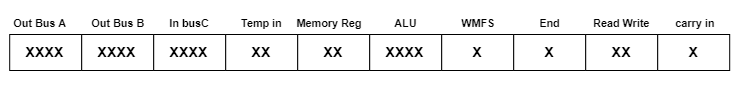
|  |  |  |  |
| --- | --- | --- | --- |
| **WMFC Selector** | | **End** | |
| **0** | **No** | **0** | **Continue** |
| **1** | **WMFC** | **1** | **End** |

|  |  |  |  |
| --- | --- | --- | --- |
| **Read Write** | | **Set ALUCarryIn** | |
| **00** | **No Operation** | **0** | **carryIn = 0** |
| **01** | **Read** | **1** | **carryIn = 1** |
| **10** | **Write** |  | |

**Micro Routines**

* **All 32 instructions are micro routines under the execution category.**
* **Fetch & Decode micro routines.**

**Micro Instruction**



**Fetch & Decode Micro Subroutine.**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **0111** | **1111** | **1111** | **00** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **0111** | **1111** | **0111** | **00** | **00** | **0000** | **1** | **0** | **00** | **1** |
| **1011** | **1111** | **1000** | **00** | **00** | **0000** | **0** | **0** | **00** | **0** |

**Fetch Source Register Mode.**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **1111** | **01** | **00** | **0000** | **0** | **0** | **00** | **0** |

**Fetch Destination Register Mode.**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **1111** | **10** | **00** | **0000** | **0** | **0** | **00** | **0** |
| **XXXX** | **1111** | **1111** | **11** | **00** | **0000** | **0** | **0** | **00** | **0** |

**Fetch Source Auto Increment.**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **1111** | **00** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **XXXX** | **1111** | **XXXX** | **00** | **00** | **0000** | **0** | **0** | **00** | **1** |
| **1011** | **0000** | **0000** | **01** | **00** | **0000** | **1** | **0** | **00** | **0** |

**Fetch Destination Auto Increment.**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **1111** | **11** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **XXXX** | **0000** | **XXXX** | **00** | **00** | **0000** | **0** | **0** | **00** | **1** |
| **1011** | **1111** | **1111** | **10** | **00** | **0000** | **1** | **0** | **00** | **0** |

**Fetch Source Auto Decrement**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **XXXX** | **00** | **00** | **0011** | **0** | **0** | **00** | **0** |
| **XXXX** | **1111** | **1111** | **00** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **01** | **00** | **0000** | **1** | **0** | **00** | **0** |

**Fetch Destination Auto Decrement.**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **XXXX** | **00** | **00** | **0011** | **0** | **0** | **00** | **0** |
| **XXXX** | **1111** | **1111** | **11** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **10** | **00** | **0000** | **1** | **0** | **00** | **0** |

**Fetch Source Register Indirect**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **1111** | **00** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **01** | **00** | **0000** | **1** | **0** | **00** | **0** |

**Fetch Destination Register Indirect**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **1111** | **11** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **10** | **00** | **0000** | **1** | **0** | **00** | **0** |

**Fetch Source Auto Increment Indirect**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **1111** | **00** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **XXXX** | **1111** | **XXXX** | **00** | **00** | **0000** | **0** | **0** | **00** | **1** |
| **1011** | **1111** | **1111** | **00** | **10** | **0000** | **1** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **01** | **00** | **0000** | **1** | **0** | **00** | **0** |

**Fetch Destination Auto Increment Indirect**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **1111** | **00** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **XXXX** | **1111** | **XXXX** | **00** | **00** | **0000** | **0** | **0** | **00** | **1** |
| **1011** | **1111** | **1111** | **11** | **10** | **0000** | **1** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **10** | **00** | **0000** | **1** | **0** | **00** | **0** |

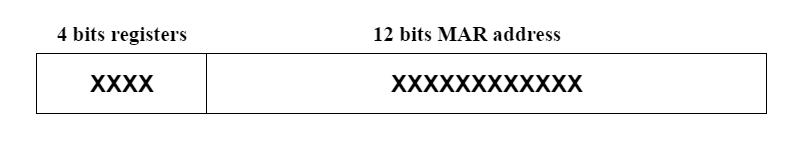
**Fetch Source Auto Decrement Indirect**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **XXXX** | **00** | **00** | **0011** | **0** | **0** | **00** | **0** |
| **XXXX** | **1111** | **1111** | **00** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **00** | **10** | **0000** | **1** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **01** | **00** | **0000** | **1** | **0** | **00** | **0** |

**Fetch Destination Auto Decrement Indirect**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **XXXX** | **1111** | **XXXX** | **00** | **00** | **0011** | **0** | **0** | **00** | **0** |
| **XXXX** | **1111** | **1111** | **00** | **10** | **0000** | **0** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **11** | **10** | **0000** | **1** | **0** | **01** | **0** |
| **1011** | **1111** | **1111** | **10** | **00** | **0000** | **1** | **0** | **00** | **0** |

**Storing Circuit ( Either Storing in Register or Storing in RAM )**



**How to store in registers**

**Decoder Enable = not( Z15 and Z14 and Z13 and Z12 ) .. if True then Don’t Write To Memory.**

**Decoder Selector ( 3 downto 0 ) = Z15 , Z14 , Z13 , Z12.**

**All the time MAR will be loaded with ( Z10 downto 0 ).**

**All the time MDR will be loaded with the data from busC.**

**Execution Micro Instructions**

**MOV**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1001** | **1010** | **If** | **00** | **01** | **0000** | **0** | **0** | **if** | **0** |

**Add**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1001** | **1010** | **If** | **00** | **01** | **0001** | **0** | **0** | **if** | **0** |

**ADC**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1001** | **1010** | **If** | **00** | **01** | **0001** | **0** | **0** | **if** | **1** |

**SUB**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1001** | **1010** | **If** | **00** | **01** | **0010** | **0** | **0** | **if** | **1** |

**SUBC**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1001** | **1010** | **If** | **00** | **01** | **0010** | **0** | **0** | **if** | **0** |

**AND**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1001** | **1010** | **If** | **00** | **01** | **0100** | **0** | **0** | **if** | **0** |

**OR**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1001** | **1010** | **If** | **00** | **01** | **0101** | **0** | **0** | **if** | **0** |

**XNOR**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1001** | **1010** | **If** | **01** | **00** | **0110** | **0** | **0** | **if** | **0** |
| **1001** | **1111** | **If** | **00** | **01** | **0111** | **0** | **0** | **if** | **0** |

**CMP**

**INC**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **0000** | **0** | **0** | **if** | **1** |

**DEC**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **0011** | **0** | **0** | **if** | **0** |

**CLR**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **0011** | **0** | **0** | **if** | **1** |

**INV**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **0111** | **0** | **0** | **if** | **0** |

**LSR**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **1000** | **0** | **0** | **if** | **0** |

**ROR**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **1001** | **0** | **0** | **if** | **0** |

**RRC**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **1010** | **0** | **0** | **if** | **X** |

**ASR**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **1011** | **0** | **0** | **if** | **0** |

**LSL**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **1100** | **0** | **0** | **if** | **0** |

**ROL**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **1101** | **0** | **0** | **if** | **0** |

**RLC**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1101** | **1111** | **If** | **00** | **10** | **0000** | **0** | **0** | **00** | **0** |
| **1010** | **1111** | **If** | **00** | **01** | **1110** | **0** | **0** | **if** | **0** |

**HLT**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1111** | **1111** | **1111** | **00** | **00** | **0000** | **1** | **0** | **00** | **0** |

**NOP**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1111** | **1111** | **1111** | **00** | **00** | **0000** | **0** | **0** | **00** | **0** |